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(71)Applicant : HITACHI LTD

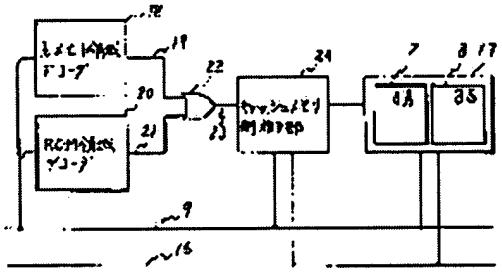
(72)Inventor : ITO HIROMICHI

(54) INFORMATION PROCESSING METHOD AND DEVICE THEREFOR

(57)Abstract:

PURPOSE: To provide an information processor containing a storage which decides a ROM storing a system starting program, a basic input/output program, etc., as a copying object to a cache memory and then attains the fast accesses to the data, etc., of the ROM.

CONSTITUTION: An information processor contains a cache memory 17, a main memory, and a ROM which stores at least a basic input/output program. Then a means is added to the information processor to store the copy of information stored in at least a part of the ROM into the memory 17, together with a means which inhibits the updating of the information stored in the memory 17 and sent from the ROM when an updating access is tried to the information. In such a constitution, the ROM storing a system starting program, a basic input/ output program, etc., is decided as a copying object to the memory 17. Then the fast accesses are possible to the data, etc., stored in the ROM.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the storage in an information processor, and relates to a cache memory control system suitable when it has ROM and cache memory especially.
[0002]
[Description of the Prior Art] It considers as a means to accelerate seemingly the data access from a central processing unit (CPU) to the main memory of low-speed large capacity, and there is an approach using the cache memory of a high-speed smallness capacity. By this approach, memory access of CPU is performed to the cache memory to which some data of main storage are copied first, and only when the data for which it asks do not exist in cache memory, access to main memory is performed. If the suitable data on main memory are copied to cache memory, only access to the almost high-speed cache memory of the data access from CPU can be made to require in the usual program, since locality is in a data access.
[0003] An example of the configuration of the direct map method (it is also called a KONGURUENTO method) of cache memory which is a formula on the other hand is shown in drawing 2 .
[0004] Cache memory 17 consists of two of AA (address Ares and Address Array)2 the address tags whose data of BS (a buffer storage, Buffer Storage)3 and BS3 with which the copy of data of main memory 4 is memorized are the information which shows whether it is data of the address of main memory 4 throat are remembered to be. Addressing of AA2 and BS3 is carried out by the lower bit section 10 among the addresses 9 which CPU1 outputs. On the other hand, the remaining high-order-bit section 11 is memorized to AA2 as an address tag 12. A comparator 5 compares the address tag 12 read from the address high-order-bit section 11 and AA2 at the time of the memory access of CPU1. A mistake hit, a call, and this information are outputted from a comparator 5 as hit information 13 in the case where did not hit the case where the result of said comparison was in agreement, and it is not in agreement.
[0005] When it hits at the time of a memory lead (it is henceforth called a lead hit), using the hit information 13, a data selector 7 chooses the BS data 14, and sends data to CPU1 through a data bus 16. When a mistake hit is carried out at the time of a memory lead (it is henceforth called a lead mistake hit), using the hit information 13, a data selector 7 chooses the main memory data 15, and sends data to CPU1 through a data bus 16. Furthermore, while copying the main memory data 15 to BS3 through a data buffer 8 at the time of a lead mistake hit, the high-order-bit section 11 of the address is written in AA2 through an address buffer 6.
[0006] On the other hand, in order to maintain coincidence of the contents of BS3 and the contents of main memory 4 at the time of a memory light, actuation shown below is performed. When it hits at the time of a memory light (it is henceforth called a light hit), the contents of both BS3 and the main memory 4 are updated. When a mistake hit is carried out at the time of a memory light (it is henceforth called a light mistake hit), only main memory 4 is updated.
[0007] in addition -- as the method of the information processor using such cache memory -- Information Processing Society of Japan -- it is discussed in Vol.21 and No.4(Apr.1980) PP 332-340 "cache storage."
[0008] Usually in the room of CPU1, ROM (Read Only Memoly), an I/O (Input/Output) device, etc. are mapped other than the main memory which is a candidate for a copy to cache memory. In access of CPU1 to the device of the outside for a copy, cache memory is bypassed and these devices are accessed

directly. For example, in the cache controller 82385 of U.S. Intel, an input terminal called NCA (Non-Cacheabel Access) is prepared, and, thereby, cache memory can be bypassed now. Said cache controller is stated to 82385 data sheets 290143-001 of the U.S. Intel issue, and pp17 in detail.
[0009] The situation of renewal of the cache memory in access out of the copy object domain to cache memory and a copy object domain is shown in drawing 3 .
[0010]
[Problem(s) to be Solved by the Invention] A program, an intercalation output program, etc. for system starting are memorized by ROM. Moreover, although accessing from CPU1 is common after transmitting a usual program and data to main memory from magnetic storage etc., they can make said transfer unnecessary by memorizing such information to ROM.
[0011] However, with the above-mentioned conventional technique, the address field of ROM has become the outside for [to cache memory] a copy, and there was a problem that the program or data on ROM could not be accessed at a high speed using cache memory.
[0012] The purpose of this invention is to offer the information processor which made the address field of ROM the copy object domain to cache memory, and made access to ROM the high speed seemingly.
[0013] Other purposes of this invention are to offer the updating approach of cache memory which an inequality does not produce between the contents of the ROM, and the contents of the cache memory to which these contents are copied.
[0014] The purpose of further others of this invention is to offer the information processor which can do main memory, ROM, or both for [to cache memory] a copy if needed.
[0015] The purpose of further others of this invention is to offer the main memory check method which accelerated the check of main memory using cache memory.
[0016]
[Means for Solving the Problem] The purpose of this invention is attained by copying the read-out data from ROM to cache memory at the time of the read access to a ROM field.
[0017] Other purposes of this invention are attained by not updating the contents of cache memory or repealing the contents of cache memory, even if cache memory hits at the time of light access to ROM.
[0018] Other purposes of this invention establish the register which sets up the copy object domain to cache memory, a means to decode a main memory field, and a means to decode a ROM field, and are attained by determining whether consider as the copy object domain to cache memory based on the set point and the above-mentioned decoding result of the above-mentioned register.
[0019] Other purposes of this invention are attained during the check of main memory by not making a main memory field into the copy object domain to cache memory, but making a ROM field into the copy object domain to cache memory.
[0020]
[Function] If cache memory carries out a mistake hit at the time of the read access to ROM by making the address field of ROM into the copy object domain to cache memory, the read-out data from ROM will be copied to cache memory. Since the copied data can be read from high-speed cache memory, without accessing ROM, they can make access to ROM a high speed seemingly.
[0021] Moreover, the inequality of the contents does not arise between ROM from which the contents do not change even if it performs light access, and the cache memory to which the contents of this ROM are copied by not updating the contents of cache memory, even if cache memory sets at the time of light access to a ROM field. Or when cache memory hits at the time of light access to a ROM field, access next to the address which performed said light access surely serves as a mistake hit by repealing the contents of cache memory. In order to access ROM directly in a mistake hit, there is nothing from which the contents of the ROM field changed with light accesses and that is looked like from CPU.
[0022] Moreover, it sets whether the copy object domain to cache memory is made only into a main memory field, it is made only into a ROM field, or it carries out to both a main memory field and a ROM field to the register which sets up the copy object domain to cache memory. On the other hand, the address is decoded with a means to decode a main memory field, and a means to decode a ROM field, and when it is a main memory field or a ROM field, the set point of said register determines whether it is a copy object domain to cache memory.
[0023] Moreover, in case the read/write check of main memory is performed, a main memory field is made into the outside for [to cache memory] a copy, and makes applicable [to cache memory] to a copy the field of ROM where the checking program is stored. Direct access of the main memory can be carried out by this, and a checking program can access a high speed using cache memory.

[0024]
[Example] Hereafter, one example of this invention is explained, referring to a drawing. In this example, as shown in drawing 4 , the room of CPU1 is 16MB (M= 220), among these 1MB of 0FFFFFH address is assigned to a main memory field from 000000H street (H of a tail expresses a hexadecimal with the abbreviation for HEX), and 64KB (K= 210) of a FFFFFFH address is assigned to the ROM field from FF0000H street, respectively. The block diagram of this example is shown in drawing 5 . The main memory field decoder 18 decodes the value of the address 9, and when it is the main memory field of 000000H - 0FFFFH, it activates the main memory field signal 19. The ROM field decoder 20 decodes the value of the address 9, and when it is the ROM field of FF0000 H-FFFFFFH, it activates the ROM field signal 21. If OR gate 22 has active one of the main memory field signal 19 and the ROM field signals 21, it will activate the copy object domain signal 23. The cache memory control section 24 controls renewal of AA2 and BS3 which constitute cache memory 17 as shown in drawing 3 according to the copy object domain signal 23. The description of this example is having made the ROM field into the copy object domain to cache memory 17.
[0025] Drawing 6 is the block diagram of the 2nd example of this invention. The description of this example is having added AND gate 25 to the 1st example. The ROM field signal 21 outputted from the ROM field decoder 20 and the RD signal 27 which shows that it is read access are inputted into AND gate 25. Both AND gates 25 activate the ROM field lead signal 26, when two inputs are active. OR gate 22 activates the copy object domain signal 23, when the main memory field signal 19 or the ROM field lead signal 26 is active. Thereby, in light access to a ROM field, the copy object domain signal 23 does not become active. The renewal of AA2 and BS3 which the cache memory control section 24 performs based on said copy object domain signal 23 is shown in drawing 1 R> 1. As shown in drawing 1 , even if it hits in light access to a ROM field, the contents of BS3 are eternal and consistency with ROM from which the contents do not change with light accesses is maintained.
[0026] Drawing 7 is the block diagram of the 3rd example of this invention. V bit 31 which shows the effectiveness of each contents of AA2 is added to AA2. The copy object domain signal 23 to cache memory is acquired like the 1st example by inputting the main memory field signal 19 and the ROM field signal 21 into OR gate 22. On the other hand, the ROM field signal 21 and the WT signal 29 which shows that it is light access are inputted into AND gate 28, and the ROM field light signal 30 is acquired. V bits of cache memory control sections 24 are set as the value which is added to the contents of AA2 by which the ROM field light signal 30 is referred to by said light access to active light access and which shows an invalid for 31. Since 31 [V-bit] is an invalid when this leads at a degree the address which performed the above-mentioned light access, it is treated as a mistake hit. Since the direct reference of the ROM is carried out in a lead mistake hit, the contents of BS3 updated when it hits in the above-mentioned light access are not referred to.
[0027] Drawing 8 is the block diagram showing the 4th example of this invention. The description of this example is having formed the register 32 which sets up the copy object domain to cache memory in addition to the 2nd example shown by drawing 6 . A register 32 has 34 [M-bit / R-bit] with 33, and corresponds to a main memory field and a ROM field, respectively. CPU1 performs a setup to this register 32 using the address 9 and the bus of data 16. M bits of R bits of values of 34 are outputted with the value of 33, respectively as the main memory field enable signal 35 and a ROM field enable signal 36. When both the main memory enable signal 35 and the main memory field signal 19 are active, AND gate 37 activates the main memory copy signal 38. Similarly, when both the ROM field enable signal 36 and the ROM field lead signal 26 are active, AND gate 39 activates the ROM copy signal 40. And when the main memory copy signal 38 or the ROM copy signal 40 is active, OR gate 22 activates the copy object domain signal 23. Thereby, the reference and updating of cache memory at the time of access to a main memory field or a ROM field can be independently permitted or forbidden about each field.
[0028] Drawing 9 is a flow chart which performs the memory check of main memory 4 with an information processor including the 4th example shown by drawing 8 . First, in advance of the memory check of main memory 4, "0" is set as M bit 33 of a register 32, and "1" is set as 34. [R-bit] Thereby, only a ROM field turns into a copy object domain to cache memory. Next, a read/write check is performed to main memory 4. Since the main memory field has become the outside for a copy at this time, direct read/write of the main memory 4 can be carried out.
[0029] Moreover, by putting the read/write checking program into ROM used as the copy object domain to cache memory, a program can be referred to at a high speed and the check of main memory 4 can be ended by short time amount.

[0030] This invention does not remain only in the example described above. For example, the address of a ROM field and a main memory field may not be the address shown in the example. Moreover, as a method of cache memory, not only a direct map method but a set ASOSHIATIBU method etc. may be used. Moreover, a write-through method or a copy back method is sufficient as the write-in method at the time of a light.
[0031]
[Effect of the Invention] According to this invention, the program and data which were memorized by ROM can be accessed at a high speed using cache memory.
[0032] Moreover, according to this invention, even if light access to a ROM field is performed, an inequality does not arise between the contents of the ROM, and the contents of cache memory.
[0033] moreover -- according to this invention -- the copy object domain to cache memory -- one side of a ROM field and a main memory field -- or it can set up and change into both easily.
[0034] Moreover, according to this invention, the program on ROM can perform a main memory check at a high speed.

[Translation done.]